In the Claims

1. A method for managing multiple memory devices over a range of logical addresses, the method comprising:

receiving a command comprising a first logical address from the range of logical addresses;

determining a first physical address, from a range of physical addresses, that corresponds to the first logical address; and

generating a chip select signal in response to the first physical address.

2. The method of claim 1 wherein the range of physical addresses is contiguous.

3. The method of claim 1 wherein the range of physical addresses is substantially equivalent to the range of logical addresses.

4. The method of claim 1 wherein the multiple memory devices are flash RAM devices.

5. The method of claim 1 wherein the range of logical addresses are contiguous and the corresponding range of physical addresses is non-contiguous and comprised of a plurality of physical address sub-ranges.

6. The method of claim 5 wherein a chip select signal is generated for each physical address sub-range.

7. A method for managing multiple flash memory devices over a range of logical addresses, the method comprising:

receiving a command comprising a first logical address from the range of logical addresses;

determining a first physical address, from a range of non-contiguous physical addresses, that corresponds to the first logical address; and

generating a chip select signal in response to the first physical address.

8. The method of claim 7 wherein receiving the command comprises a controller circuit executing an application in which the first logical address is read from memory along with the command.

9. The method of claim 7 wherein receiving the command comprises a device manager receiving the first logical address from a controller circuit.

10. The method of claim 9 wherein the device manager generates the chip select signal in response to the first physical address.

11. A method for managing multiple flash memory devices over a range of logical addresses, the method comprising:

a controller circuit executing an application;

the controller circuit receiving a first logical address from the range of logical addresses in response to the execution of the application;

determining a first physical address, from a range physical addresses comprising a plurality of non-contiguous sub-ranges, that corresponds to the first logical address;

outputting the first physical address to chip select generation circuitry; and

the chip select generation circuitry generating a chip select signal in response to the first physical address.

12. The method of claim 11 wherein each of the plurality of non-contiguous sub-ranges is substantially equal to a logical address range of a flash memory device of the multiple flash memory devices.

13. An electronic system having a logical address map comprising a flash memory logical address range for a designed memory device, the system comprising:

a plurality of flash memory devices having a combined physical address range substantially equivalent to the flash memory logical address range;

a controller circuit coupled to the plurality of memory devices, the controller circuit capable of generating a first physical address from the combined physical address range in response to a first logical address received from an executing software application; and

a chip select generation circuit coupled to the controller circuit and the plurality of memory devices, the chip select generation circuit transmitting a chip select signal to one of the plurality of memory devices in response to the first physical address.

14. The system of claim 13 wherein the controller circuit is coupled to the plurality of flash memory devices through a plurality of address lines.

15. The method of claim 13 wherein the controller circuit generates the first physical address in response to a look-up table entry comprising the first logical address and the first physical address.

16. The method of claim 13 wherein the controller circuit generates the first physical address in response to adding an address offset to the first logical address.

17. An electronic system having a logical address map comprising a flash memory logical address range for a designed memory device, the system comprising:

a processor that executes a software application, thereby generating a first logical address;

a plurality of flash memory devices having a combined physical address range substantially equivalent to the flash memory logical address range, the plurality of flash memory devices coupled to the processor over address lines; and

a device manager coupled to the plurality of flash memory devices and the processor, the device manager comprising:

a controller function capable of generating a first physical address from the combined physical address range in response to the first logical address; and

a chip select generation function capable of transmitting a chip select signal to one of the plurality of memory devices in response to the first physical address.

18. The electronic system of claim 17 wherein the controller function uses a look-up table stored in memory to generate the physical address in response to the logical address.

19. The electronic system of claim 17 wherein the controller function adds an address offset to the logical address to generate the physical address.

20. In an electronic system that is controlled by a processor, a method for managing multiple flash memory devices over a range of logical addresses, the method comprising:

the processor executing a software application;

the processor receiving a first logical address from the range of logical addresses in response to the execution of the application;

the processor determining a first physical address, from a range physical addresses comprising a plurality of non-contiguous address sub-ranges, that corresponds to the first logical address;

the processor outputting the first physical address to chip select generation circuitry; and

the chip select generation circuitry transmitting a chip select signal, generated in response to the first physical address, to a first flash memory device of the multiple flash memory devices.